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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Louis L. Hsu

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7590

10/18/2004

EXAMINER

NGUYEN, DANNY

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ART UNIT

PAPER NUMBER

2836

DATE MAILED: 10/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/929,591

Applicant(s)

HSU ET AL.

Examiner

Danny Nguyen

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AN

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 July 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 10, 11, 20 and 22 is/are allowed.
- 6) ☒ Claim(s) 1-9, 12-19, 21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1, 12 have been fully considered, but they are not persuasive.

Regarding claim 1, applicant argued that Keeth does not disclose a plurality of internal voltage supply generators, each is connected to a respective macro of the plurality of macros and configured for receiving the external voltage, generating an internal voltage, and using the generated internal voltage supply ^{for} ~~for~~ operating its respective macro. The argument is not convincing because Keeth does teach that a plurality of internal voltage supply generators (such as a plurality of internal voltage supply generators 804(1) to 804(8)), each is connected to a respective macro (each of the plurality of voltage generators 804(1) to 804(8) is connected to each macro 802) of the plurality of macros (802(1) to 802(8)) and configured for receiving the external voltage (such the external voltage supply Vcc), generating an internal voltage, and using the generated internal voltage supply ^{for} ~~for~~ operating its respective macro (e.g. col. 8, lines 44-50). Thus applicant's arguments with respect to claim 1 do not distinguish over Keeth reference. Claims 1-9 remain rejected.

Regarding claim 12, applicant argued that Keeth does not disclose second means for generating an internal voltage, and using the generated internal voltage supply for operating at least one of a plurality of internal voltage supply generators coupled a respective macro of the plurality of the macros, the second means is coupled

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to the first means. The argument is not persuasive because Keeth does teach second means (such as 804) for generating an internal voltage, and using the generated internal voltage supply for operating at least one of a plurality of internal voltage supply generators coupled ^{to} a respective macro of the plurality of the macros (802), the second means (804) is coupled to the first means (Vcc) (e.g. col. 8, lines 44-50, col. 9, lines 55-60, col. 10, lines 55-60). Claims 12-19, 21 remain rejected.

Regarding claims 1 and 12, applicant argued that Keeth does not disclose at least one enable/disable circuit for selectively connecting and disconnecting at least one portion of the respective macro from the integrated circuit system and means for controlling the second means according to an enable/disable signal to selectively connect and disconnect at least a portion of the respective macro of the plurality of macros. However, Keeth discloses enable/disable circuit for selectively connecting and disconnecting at least one portion of the respective macro from the integrated circuit system (e.g. see col. 3, lines 55-59) and means for controlling the second means according to an enable/disable signal to selectively connect and disconnect at least a portion of the respective macro of the plurality of macros (col. 8, 50-54, col. 9, lines 55-60, col. 10, lines 55-60). Claims 1-9 and 12-19 remain rejected.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

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A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5, and 12-15, 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Keeth (USPN 5,946,257).

Regarding claims 1, 2, Keeth discloses an integrated circuit system (see fig. 1 and 8) having a plurality of macros (memory arrays 801(1) to 801(8)), the integrated circuit comprises an external voltage supply input (the external supply input voltage Vcc) configured to supply an external voltage to the integrated circuit; and a plurality of internal voltage supply generators (e.g. 804 (1) to 804 (8)), each connected to a respective macro and configured for receiving the external voltage for generating an internal voltage supply for operating its respective macro (e.g. col. 9, lines 55-60), and each of the plurality of internal voltage supply generators including at least one supply circuitry (such as circuitry shown fig. 10) for generating the internal voltage supply, at least one enable/disable circuitry. (Note that at least one circuit (819) corporate each of the plurality of voltage generators (804 (1) to 804 (8)) for individually enabling and disabling one of the plurality of memory arrays as defected is found as stated in col. 11, lines 52-55) for selectively connecting and disconnecting at least a portion of the respective macro from the integrated circuit system.

Regarding claim 12, Keeth discloses an integrated circuit system (fig. 1 and 8) having a plurality of macros (such as 802 (1) to 802 (8) shown in fig. 8) comprises first means for receiving an external voltage (Vcc), second means (e.g. voltage generators 804 (1) to 804 (8)) coupled to the means for receiving the external voltage for

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generating an internal voltage supply and using the generated internal voltage supply for operating at least one of a plurality of internal voltage supply generators coupled to a respective macro, the second means is connected to the first means, and means (such 916 of generator controller 806 shown in fig. 8 and 9) for controlling the means (such 804) coupled the second means for receiving the external voltage according an enable and disable signal to selectively connect and disconnect at least a portion of the respective macro (col. 8, 50-54, col. 9, lines 55-60, col. 10, lines 55-60).

Regarding claim 3, Keeth discloses the external voltage is greater than the internal voltage (the internal supply voltage is approximately one half of the external supply voltage V_{cc} , see col. 9, lines 9, line 58).

Regarding claims 4, 13, 21, Keeth discloses a scan-chain formed by a chain of scannable register latches storing fuse information and switch enable/disable signal (see col. 4, lines 53-57).

Regarding claims 5, 14, 15, Keeth discloses each of the plurality of internal voltage generators comprises a reference voltage generator (1004) for generating and providing a reference voltage for driving at least one voltage generator (see fig. 10).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 7-9, 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keeth in view of Sher et al. (USPN 6,496,027).

Regarding to claims 7-9, Keeth discloses a reference supply unit (1004) for generating at least one of a voltage level and current level; a voltage limiter (1002) coupled to the reference supply unit for controlling a voltage output level outputted from the voltage limiter; and a charge pump (capacitor, see fig. 10) for receiving voltage level for generating the internal voltage supply. Keeth does not disclose an oscillator and a feedback voltage provided from the charge pump. Sher et al. disclose a voltage supply generator (26) comprises an oscillator (130) and a feedback voltage (see fig. 10). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the system of Keeth to incorporate an oscillator with a feedback voltage to produce the internal supply voltage to the memory arrays (col. 6, lines 5-19).

Claim 11 repeats limitations of claim 4; therefore, it is rejected accordingly.

Claims 17-19 repeat limitations of claims 7-9; therefore, they are rejected accordingly.

4. Claims 6, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keeth in view of Hsu et al (USPN 6,343,044). Keeth discloses all limitations of claims 1 and 12 except for having a substrate bias level generator, a negative word line level voltage generator, and a boosted high level voltage generator. Hsu discloses a memory (e.g. fig. 3) comprises a substrate bias level generator (V_{bb}), a negative word line level voltage generator (V_{wl}), and a boosted high level voltage generator (V_{pp}) (see col. 1, lines 10-42 and col. 5, lines 45-46). It would have been obvious to one of ordinary skill

in the art at the time the invention was made to have modified the system of Keeth to incorporate a Vbb generator, a Vwl generator, and a Vpp generator as taught by Hsuan in order to reduce cell leakage and improve the retention time (e.g. col. 1, lines 15-16).

Allowable Subject Matter

5. Claims 10, 11, 20, 22 are allowed.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Danny Nguyen whose telephone number is (571)-272-2054. The examiner can normally be reached on Mon to Fri 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571)-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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10/5/2004



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